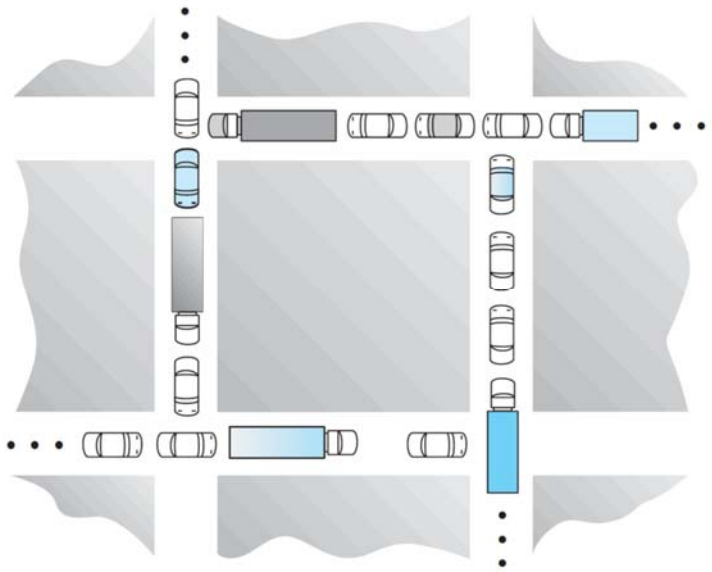
CSE 4300 Homework 3 (Due on November 17th, 2019)

Question 1 (20 points): Consider the traffic deadlock depicted in the following figure.

Question 1.1: Show that the four necessary conditions for deadlock hold in this example.

Question 1.2: State a simple rule for avoiding deadlocks in this system.



Question 2 (20 points): A system has four processes and five allocable resources. The current allocation and request matrix are as follows:

	Current Allocation Matrix
Process A	1 0 2 0 1
Process B	2 0 1 1 0
Process C	1 0 0 1 1
Process D	1 1 1 0 1

	Request Matrix
Process A	2 0 2 0 0
Process B	2 0 0 3 0
Process C	1 1 0 0 0
Process D	0 0 0 0 1

Available resources: 1 1 1 x 1

For what value of x this will be a safe state?

Show a sequence of scheduling (if exists) that will lead to successful completion of the tasks.

The request matrix specifies how many of each type of resources are still needed by each process, in addition to what it currently has.

Question 3.1 (7.5 points): Please describe the key principle of the contiguous memory allocation method. What are the hardware support for contiguous memory allocation? What are the key disadvantages of the contiguous memory allocation method?

Question 3.2 (7.5 points): Please describe the key principle of paging. What are the hardware supports for paging? What are the key advantages of paging comparing to the contiguous memory allocation method?

Question 4 (20 points): Consider a paging hardware with TLB. Assume that the TLB has a hit ratio of 0.75. Searching TLB takes 30 ns and searching memory takes 200 ns in average.

Question 4.1: What is the average cost to translate a virtual address to physical address?

Question 4.2: What is the cost if no TLB is used?

Question 5 (25 points): Consider virtual addressing of 32 bits. Assume that the page size is 8 KB. You have 16 GB of RAM.

Question 5.1: How many entries do you need in the page table?

Question 5.2: How many bits are needed to index the page table?

Question 5.3: Assume that the following table lists all the virtual pages of process A that are currently in physical memory. If a virtual page is not listed in the table, it implies that any address in that range will result a page fault and will be a miss. Translate the following virtual addresses to physical address using the table below (if possible), and mention which will be hit and which will cause a miss: 13549, 45862, 38267, 144.

Virtual Page	Physical Page
1	4
5	7
3	12
0	9