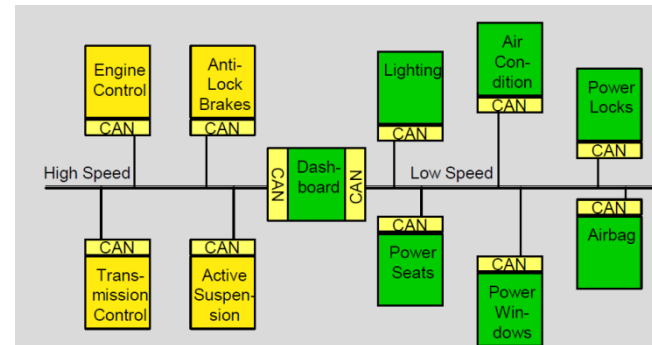
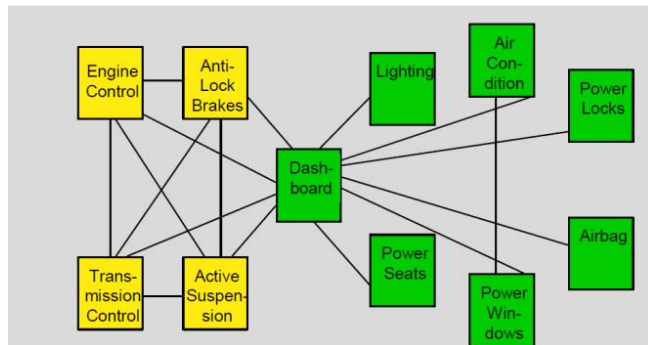
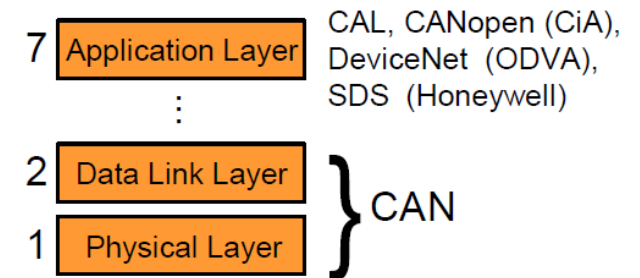


CONTROLLER AREA NETWORK (CAN)

- A multi-master bus created in early 90s by Bosch, GmbH, for use in automotive industry.
 - An open, linear structure with one logic bus line and equal nodes
 - The number of nodes is not limited by the protocol
- Source-addressing (message identifiers) with 11 bits in version A and 29 bits in version B
- Asynchronous bus access with Arbitration on Message Priority (CSMA-CD w/ AMP)
- Max payload of 8 bytes and Max data rate of 1Mbps
 - At a maximum bus length of 40m when using a twisted wire pair



CAN BUS CHARACTERISTICS: WIRED-AND

- There are two bus states, called "dominant" and "recessive".
- The bus logic uses a "Wired-AND" mechanism, that is, "dominant bits" (equivalent to the logic level "Zero") overwrite the "recessive" bits (equivalent to the logic level "One").

Two logic states possible on the bus:
"1" = recessive
"0" = dominant



A	B	C	BUS
D	D	D	D
D	D	R	D
D	R	D	D
D	R	R	D
R	D	D	D
R	D	R	D
R	R	D	D
R	R	R	R

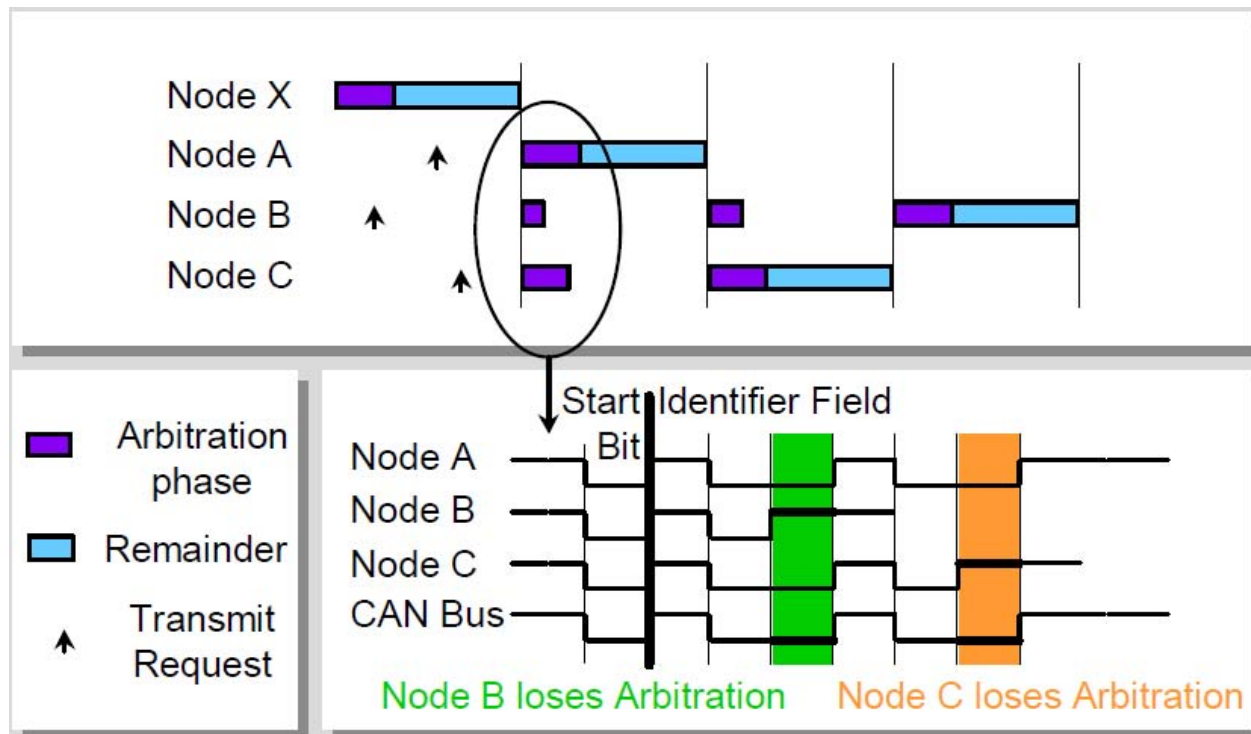
As soon as one node transmits a dominant bit (zero):
Bus is in the dominant state.

Only if all nodes transmit recessive bits (ones):
Bus is in the recessive state.

(Figure is from Siemens Microelectronics, Inc.)

BUS ACCESS AND ARBITRATION: CSMA/CD W/ AMP

- At each CAN device, the start of frame bit notifies a transmission is being sent.
- The identifier bit shows the priority of the message along with determining which device the data belongs to.
- It is not permitted for different nodes to send messages with the same identifier as arbitration could fail leading to collisions and errors.

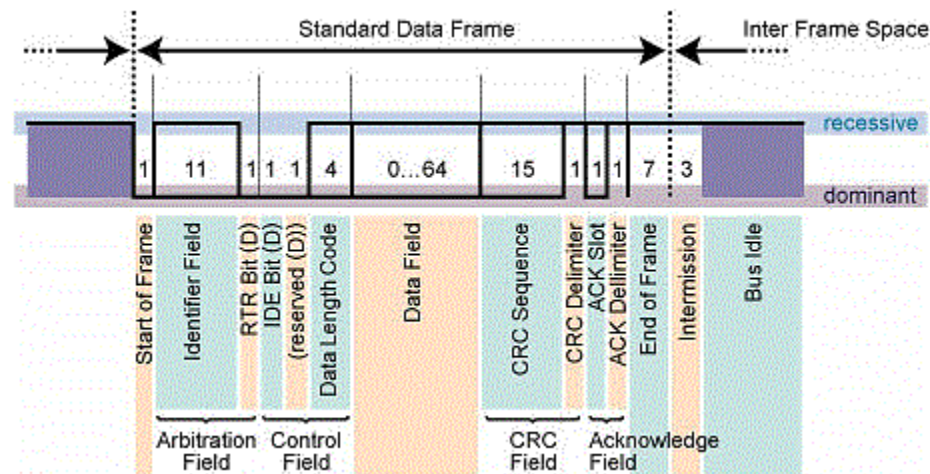


(Figure is from Siemens Microelectronics, Inc.)

CAN 2.0A MESSAGE FRAME

- Data Frame

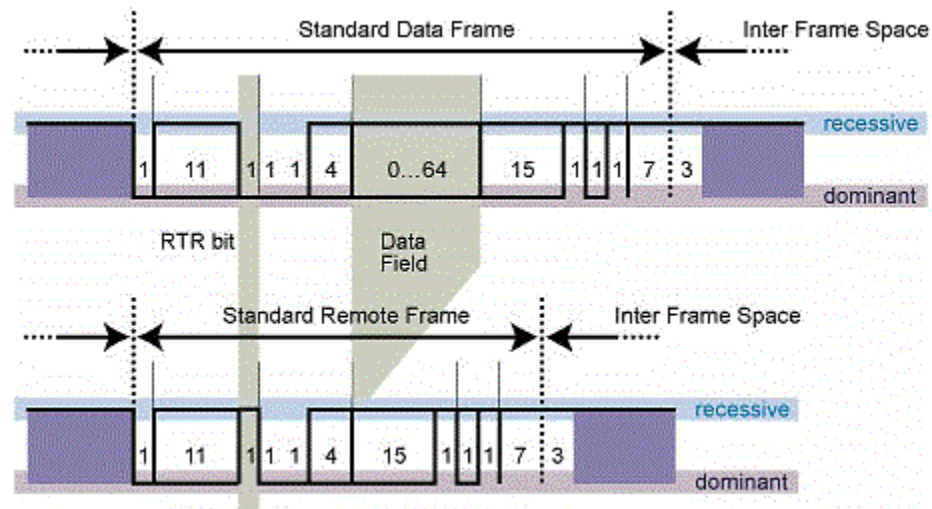
- Begins with a dominant SOF bit for hard synchronization of all nodes.
- IDE, RTR and reserved bits are set dominant.
- In the ACK Slot bit the TX node sends out a recessive bit. Any node that has received an error free frame ACKs the correct reception of the frame by sending back a dominant bit.



CAN 2.0A MESSAGE FRAME

- Remote Frame

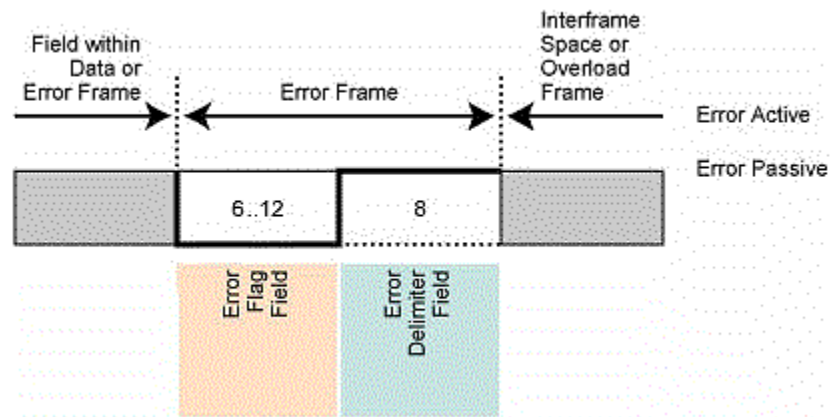
- A destination node requests the data from the source by sending a Remote Frame with an identifier that matches the identifier of the required Data Frame.
- The data source node will then send a Data Frame as a response to this remote request.
- RTR bit is set recessive and there is no Data Field.



CAN 2.0A MESSAGE FRAME

- Error Frame

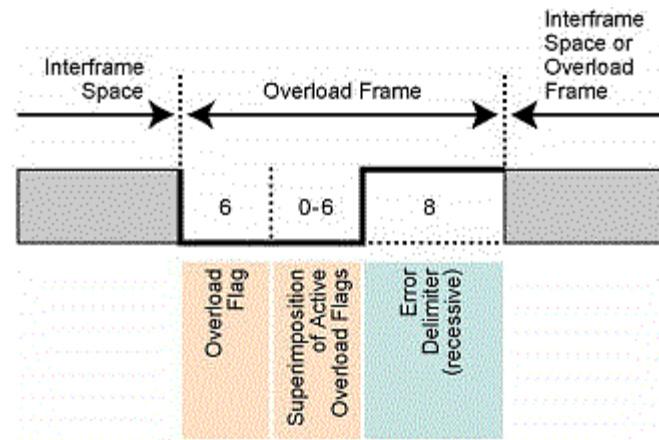
- Generated by any node that detects a bus error.
- Consists of 2 fields, an Error Flag field followed by an Error Delimiter field (8 R bits).
- “Error-active” node interrupts current transmission by generating an “active error flag” (6 D bits).
- “Error passive” node transmits an “passive Error Flag” (6 R bits).



CAN 2.0A MESSAGE FRAME

- Overload Frame

- Same format as an “active” Error Frame.
- Can only be generated during Interframe Space. Used to delay next CAN message



ERROR DETECTION MECHANISMS IN THE CAN PROTOCOL

- **Cyclic Redundancy Check (CRC)**
 - An Error Frame to request retransmission of the garbled frame.
- **Acknowledge Check**
 - An Acknowledge Error occurred when no other nodes on the bus received the frame correctly
- **Frame Check**
 - A Form Error occurred is a transmitter detects a dominant bit in one of the four segments: CRC Delimiter, Acknowledge Delimiter, End of Frame or Interframe Space.
- **Bit Monitoring**
 - All nodes perform Bit Monitoring: A Bit Error occurs if a transmitter 1) sends a D bit but detects a R bit on the bus line or, 2) sends a R bit but detects a D bit on the bus line.
- **Bit Stuffing Check**
 - If six consecutive bits with the same polarity are detected between Start of Frame and the CRC Delimiter, the bit stuffing rule has been violated.

Error Handling: detected errors are made public to all other nodes via Error Frames. The TX of the erroneous message is aborted and the frame is repeated ASAP.